(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 February 2005 (17.02.2005)

PCT

(10) International Publication Number
WO 2005/015251 A1

(51) International Patent Classification[7]: G01R 31/3185

(21) International Application Number: PCT/EP2003/050307

(22) International Filing Date: 15 July 2003 (15.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: AGILENT TECHNOLOGIES, INC. [US/US]; 395 Page Mill Road, Palo Alto 94306 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: HEINEN, Martin [DE/DE]; Baeckergaessle 7, 71149 Bondorf (DE). MOLL, Joachim [DE/DE]; Regenstrasse 5, 71083 Herrenberg (DE).

(74) Agent: BARTH, Daniel; Agilent Technologies Deutschland GmbH, Patentabteilung, Herrenberger Str. 130, 71034 Böblingen (DE).

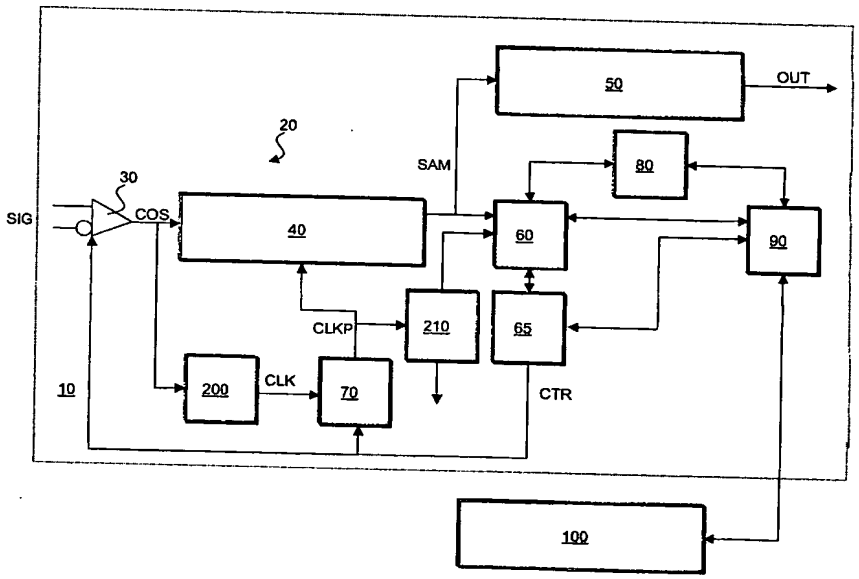
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: INTEGRATED CIRCUIT WITH BIT ERROR TEST CAPABILITY



(57) Abstract: An integrated circuit (10), preferably a field programmable gate array - FPGAor an application specific integrated circuit - ASIC -, comprises a level comparator (30) for comparing a level of a comparator input signal and correspondingly providing a comparator output signal (COS). A sampling unit (40) is coupled to the level comparator (30) for sampling (SAM) the comparator output signal (COS). A bit error test unit (60) receives the sampled comparator output signal (SAM) and determine therefrom an indication of a bit error in a sequence of the sampled comparator output signal (SAM).

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